***HLS Assignment 1(KANEKAL KOUSAR[FWC2022063])***

Q) Design an 8bit \* 8bit multiplier using HLS. There will be two 8bit inputs (use char data type) and one 16bit output (use short data type). Use ap\_none interface for the port interfaces. Write an HLS testbench to verify the output of the design. Pass 10 pair of input values to design and collect the output, and display inputs and outputs as part of the testbench. Verify if your design is working using C simulation first. Run HLS synthesis. Now, verify the design again using C/RTL co-simulation. Report your design and tb code, C simulation printed outputs, HLS resource consumption, HLS timing report, and C/RTL cosimulation printed outputs

***code:***

*1)header file*

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| **#ifndef** MUL  **#define** MUL  **#include** <stdio.h>  **#define** N 10  **typedef** **char** dinA; //8-bit  **typedef** **char** dinB; //8-bit  **typedef** **short** dout; //16-bit  **#endif** |

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| **# include** "mul2.h"  **void** **mul\_8**(dinA A,dinB B,dout \*C)  {  \*C=A\*B; //multiplier  } |

2)c code

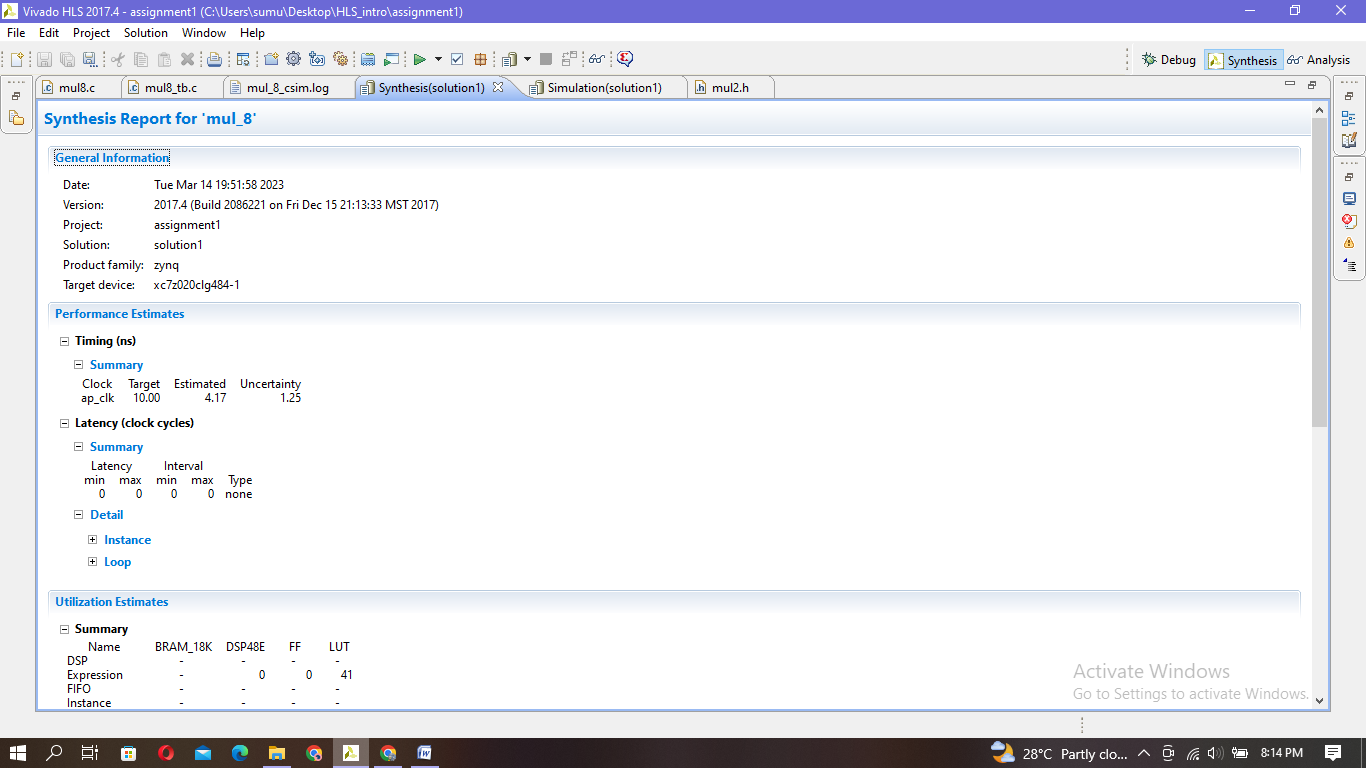
3)test-bench

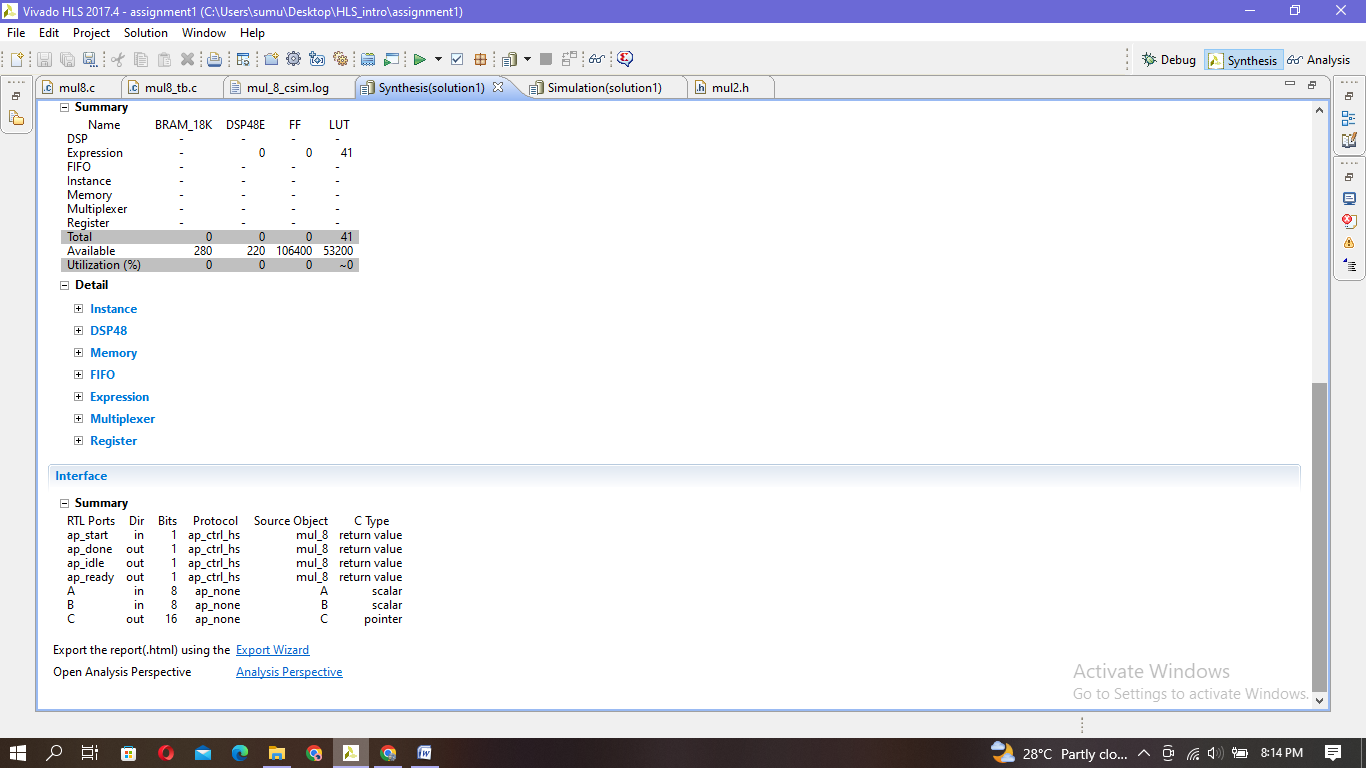
|  |
| --- |
| **# include** "mul2.h"  **int** **main**(){  dinA a;  dinB b;  dout c;  **int** i;  **for** (i=0;i<N;i++){  //creating input data  a=i+4;  b=i+5;  mul\_8(a,b,&c);  **printf**("%dX%d=%d\n",a,b,c);  }  } |

4)simulation report

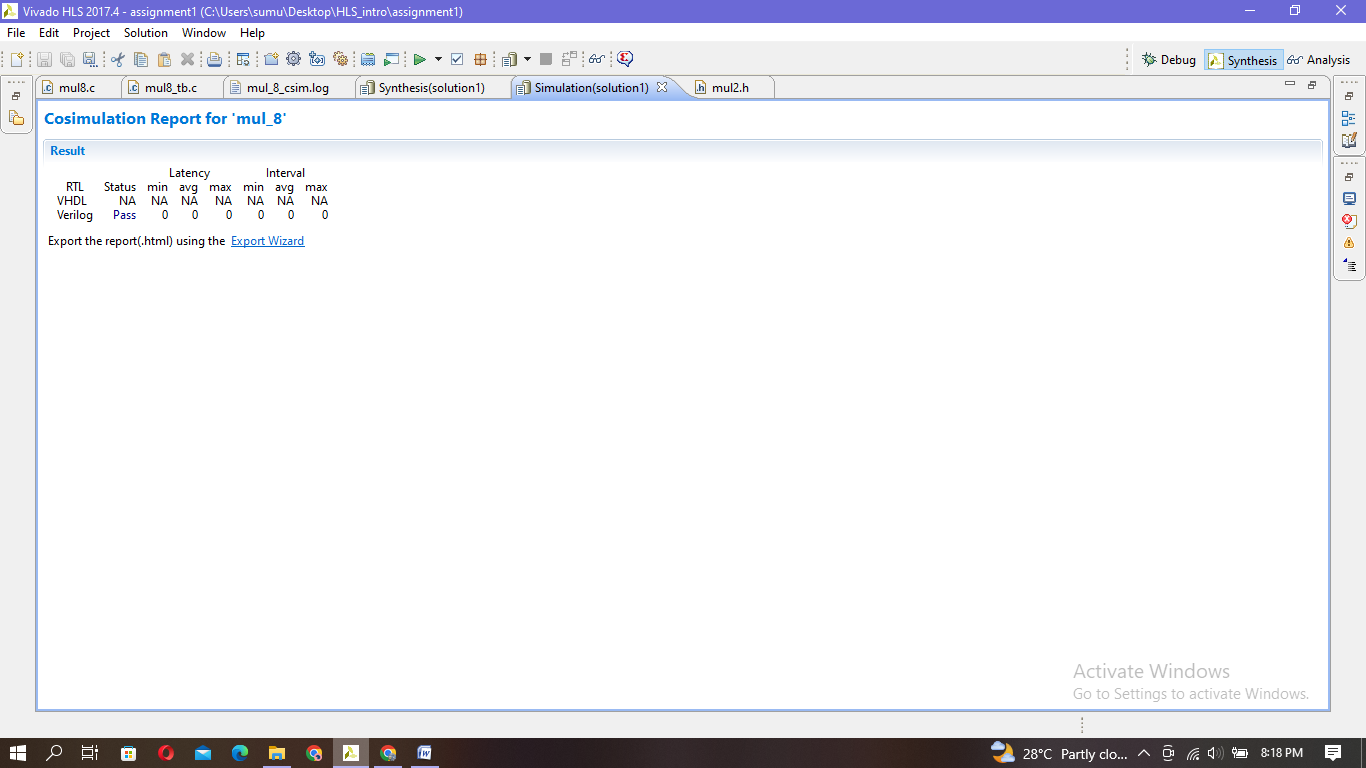
|  |
| --- |
| Screenshot (289).png |

5)synthesis report





6)co-simulation output and report



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| INFO: [Common 17-206] Exiting xsim at Wed Mar 15 14:14:39 2023...  INFO: [COSIM 212-316] Starting C post checking ...  4X5=20  5X6=30  6X7=42  7X8=56  8X9=72  9X10=90  10X11=110  11X12=132  12X13=156  13X14=182  INFO: [COSIM 212-1000] \*\*\* C/RTL co-simulation finished: PASS \*\*\*  INFO: [COSIM 212-210] Design is translated to an combinational logic. II and Latency will be marked as all 0.  Finished C/RTL cosimulation. |